IN THE SPECIFICATION:

Please delete the present title of the invention and insert the following new title of the invention:

-- A MEMORY DEVICE HAVING A FLOATING GATE--.

IN THE CLAIMS:

Please cancel claims 116, 117, 121, 123, and 125 without prejudice or disclaimer of the subject matter contained therein.

Please amend claim 17, 18, 25, 28, and 112 to read as follows:

11 17. (Amended) A semiconductor memory device comprising:

a first memory comprising:

a first floating gate formed over a semiconductor substrate;

a first control gate formed over and insulated from said first floating gate,

a first impurity region and a second impurity region formed within said semiconductor substrate, wherein said first impurity region is deeper than said second impurity region;

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a second memory comprising:

a second floating gate formed over said semiconductor substrate;

a second control gate formed over and insulated from said second floating gate,

said first impurity region; and

a third impurity region formed within said semiconductor substrate, wherein said first impurity region is deeper than said third impurity region;

wherein the depth of the second and third impurity regions is not larger than 0.1 μm.

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~~18~~. (Amended) A semiconductor memory device comprising:

a first memory comprising:

a first floating gate formed over a semiconductor substrate;

a first control gate formed over and insulated from said first floating gate,

a first impurity region and a second impurity region formed within said semiconductor substrate, wherein said first impurity region is deeper than said second impurity region;

a second memory comprising:

a second floating gate formed over said semiconductor substrate;

a second control gate formed over and insulated from said second floating gate,

said first impurity region; and a third impurity region formed within said semiconductor substrate, wherein said first impurity region is deeper than said third impurity region, and

a wiring formed on and in electrical contact with said first impurity region;

wherein the depth of the second and third impurity regions is not larger than 0.1 μm.

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67 58 ~~25~~. (Amended) A semiconductor memory device comprising:

a first memory comprising:

a first floating gate formed over a semiconductor substrate;

a first control gate formed over and insulated from said first floating gate,

a first impurity region and a second impurity region formed within said semiconductor substrate, said first impurity region being deeper than said second impurity region, wherein said first impurity region is partly overlapped with said first floating gate; and

a second memory comprising:

a second floating gate formed over said semiconductor substrate;

a second control gate formed over and insulated from said second floating gate,

said first impurity region; and

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a third impurity region formed within said semiconductor substrate, said first impurity region being deeper than said third impurity region, wherein said first impurity region is partly overlapped with said second floating gate;

wherein the depth of the second and third impurity regions is not larger than 0.1 μm.

~~28~~ 89. (Amended) A semiconductor memory device comprising:

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a semiconductor substrate;

a floating gate formed over said semiconductor substrate;

a control gate formed over and insulated from said floating gate;

a first impurity region and a second impurity region formed within said semiconductor substrate, said first impurity region being deeper than said second impurity region, wherein said first impurity region is partly overlapped with said floating gate;

an interlayer insulating film formed over said semiconductor substrate, said floating gate and said control gate; and

a wiring formed on said interlayer insulating film wherein said wiring is electrically connected to said first impurity region through a hole formed in said interlayer insulating film;

wherein the depth of the second impurity region is not larger than 0.1 μm.

~~112~~ 111. (Amended) A semiconductor memory device comprising:

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a first memory comprising:

a first floating gate formed over a semiconductor substrate;

a first control gate formed over and insulated from said first floating gate,

a first impurity region and a second impurity region formed within said semiconductor substrate, wherein said first impurity region is deeper than said second impurity region;

a second memory comprising:

a second floating gate formed over said semiconductor substrate;

a second control gate formed over and insulated from said second floating gate,